2014

[This question paper contains 2 printed pages.]

Sr. No. of Question Paper : 6082 **D** **Your Roll No.....**

Unique Paper Code : 234203

Name of the Course : **B.Sc. (H) Computer Science**

Name of the Paper : Computer System Architecture (CSHT–204)

Semester : II

Duration : 3 Hours

Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question No. **1** is compulsory.
3. Attempt any **four** questions from Section B.
4. Parts of a question must be answered together.

SECTION – A

1. (a) Describe the following elements of bus design.

   (i) Bus Type (ii) Method of arbitration (5)

   (b) The memory unit of computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of 7 addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field. (5)

   (c) Convert the following arithmetic expressions from infix to reverse Polish notations.

   (i) A + B * [C * D + E * (F + G)]

   (ii) [A * {B + C * (D + E)}] / {F * (G + H)} (2+3)

   (d) Draw a flowchart explaining the functioning of basic computer which showing both instruction and interrupt cycles. (5)

   (e) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline. (5)

   (f) Explain in detail the major functions performed by I/O modules. (5)

P.T.O.

(g) Explain the following terms in context to cache memory :
(i) Hit Ratio
(ii) Locality of reference (5)

SECTION – B

2. (a) The content of PC in the basic computer is 3AF (all numbers in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. Identify the instruction that will be fetched and executed next. Show the contents of registers PC, AR, DR, AC, IR and SC in Hex for each timing signal. Show the values of E and I also. (5)

(b) List the micro operations for executing ADD and ISZ micro instructions. (2+3)

3. (a) Briefly explain with the help of a diagram the mechanism of next address generation for the micro programmed control unit. (6)

(b) Formulate a mapping procedure that provides eight consecutive micro-instructions of each routine of a typical computer. The operation code has five bits and the control memory has 2048 words. (4)

4. (a) Give the different fields of an Assembly language. Give three examples of pseudo-instruction. (2+3)

(b) An instruction stored at location 500 with its address field at location 501. The address field has value 600. A processor register R1 contains the number 300. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with Rl as the index register. (5)

5. (a) Derive an expression for a speed up factor of a k-segment instruction pipeline. Explain the functioning of a **four** segment instruction pipeline with its space-time diagram. (6)

(b) Distinguish between memory mapped I/O and the Isolated I/O. (4)

6. (a) Explain in detail about set-associative mapping with the help of example. (6)

(b) Distinguish between Hardwired and Micro-programmed control. (4)

7. (a) Explain functioning of Direct Memory Access (DMA) I/O operation with the help of block diagram. (5)

(b) Explain following addressing modes (i) Auto increment (ii) base register addressing mode. (2+3)

(300)